INTERNATIONAL JOURNAL OF ELECTRICAL ENGINEERING & TECHNOLOGY (IJEET)

ISSN 0976 – 6545(Print)
ISSN 0976 – 6553(Online)
Volume 6, Issue 4, April (2015), pp. 09-15

Journal Impact Factor (2015): 7.7385 (Calculated by GISI)
www.jifactor.com

IJEET

©IAEME

DESIGN AND ANALYSIS OF SECOND GENERATION CURRENT CONVEYOR BASED LOW POWER OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Roma Rani[1], Pankaj Rai[2], Jyoti Athiya[3]

[1,2]Department of Electrical Engineering,
B.I.T. Sindri, Dhanbad Jharkhand 828123, India

[3]Department of Electronics & Comm. Engineering
B.I.T. Sindri, Dhanbad Jharkhand 828123, India

ABSTRACT

The paper deals with current conveyor based design criteria for low power Miller operational transconductance amplifier. Its transconductance has been controlled by using second generation current conveyor (CCII), replacing input bias current (I_{bias}). Current-mode based electronics devices becoming more popular than with voltage mode. The performance is obtained through PSPICE simulations which show the usability of the proposed circuit for high frequencies. The proposed circuit is implemented using 0.35 μm AMS CMOS technology. The power consumption of proposed circuit is reduced to 2.7μW with settling time 4.4ns and achieves high 106 dB gain using 1.5V supply voltage.

Key Words: CMOS, Operational Transconductance Amplifier (OTA), CCII, Low Power

I. INTRODUCTION

The second-generation current conveyor (CCII) proposed by Sedra and Smith [1], [2] has proved to be a functional block of current conveyor. CCII circuits have been widely used in low power and high speed circuit like filter and converter. The CCII is a three terminal device derived by interconnecting the voltage a current followers. The Y terminal is a high impedance terminal while the X terminal is a low impedance one. The input voltage Vy applied across the Y terminal is conveyed to the voltage Vx across the X terminal; i.e. (Vx=Vy).

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vx \\ Ix \\ Vz \end{bmatrix}$$

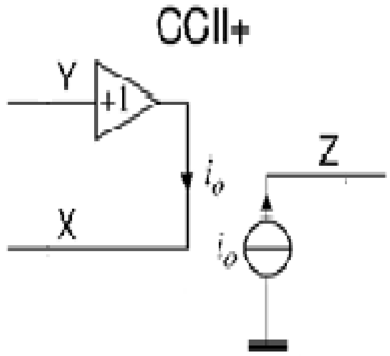

Fig.1 Matrix representation and circuit diagram of current conveyor

The OTA is a basic building block in most of analogue circuit with linear input-output characteristics, which is widely used in analog circuit such as neural networks, Instrumentation amplifier, ADC and Filter circuit. The OTA is an amplifier whose differential input voltage produces an output current. An OTA is similar to a standard operational amplifier which has a high impedance differential input stage and that it may be used with negative feedback [4],[5]. However, the threshold voltage is not reduced proportionally with the supply voltage; thus the threshold voltage is becoming a restraint for many analog circuits. Some special techniques are used to overcome the size of the threshold voltage, e.g. floating gate transistors, bulk-driven transistors and low threshold transistors.

The work focuses on the analysis, design and implementation of CMOS Miller operational Transconductance Amplifier (OTA) and Current Conveyor Based OTA. In this method, current conveyor based circuit is used replacing I_{bias}. The design procedure targeted best performance in terms of power consumption (µW), dc gain (dB), settling time(ns) and phase margin (degree) showing the best results. The process parameters were obtained through the AMS 0.35 µm CMOS technology. Current conveyor based OTA design optimizes the gain from previous [6].

This paper is organized as follows: Section 2 addresses the design concept of Miller OTA and current conveyor based OTA and its main features in detail. The Simulation results of this circuit implementation, including comparison with both circuits are shown in section 3. Finally, Section 4 presents our conclusion and future scope of this circuit.

II. 1 MILLER OTA BASED CIRCUIT REALIZATION

The basic circuit diagram of two-stage Miller CMOS differential amplifier is often desired as the first stage in an op-amp due to its differential input to single-ended output conversion and its high gain. The input devices of the differential pair are formed by P-channel MOSFETs M4 and M5. Either N-channel MOSFET (NMOS) or P-channel (PMOS) input devices can be used. However, PMOS input devices are used more often thanks to improved slew rate and reduced flicker time noise [7]. The use of PMOS input devices also provides reduced power supply rejection due to the current mirrors, and low sensitivity to change in power supply. This first stage of op-amp also had the current mirror circuit formed by an N-channel MOSFETs, M1 and M2. The transistor M3 serves as a P-channel common source amplifier which is the second stage of op-amp. The current Ibias of the op-amp circuit goes through current mirrors formed by P-channel MOSFETS, M6, M7 and M8. It is designed to produce a current of 100 µA.

Transistor	W /L(μm)
M1,M2	10/1
M4,M5	24/1
M6,M7	41/1
M8	220/1
M3	148/1

Table 1: Miller OTA transistor dimensions

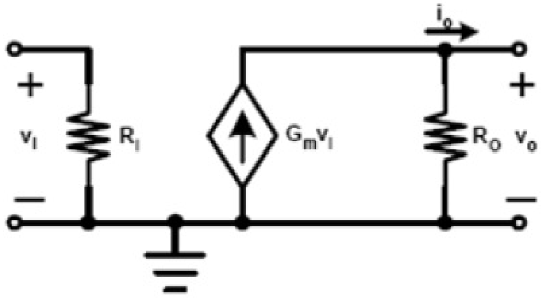

Fig.2 Equivalent circuit Diagram of OTA

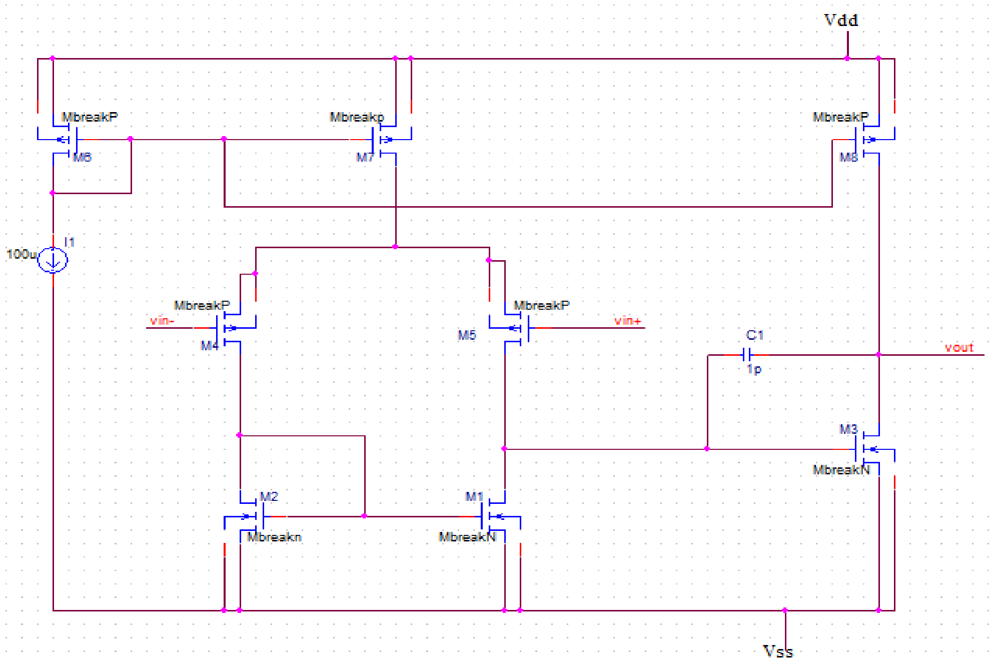

Fig.3 Miller OTA based circuit

II. 2 PROPOSED CURRENT CONVEYOR BASED OTA CIRCUIT REALIZATION

The CCII + [1], [2] structure begins with the differential input wide range transconductance amplifier. The CMOS realization of current conveyor based OTA circuit shown in Fig 4; consists of CCII+ circuit in place of I_{bias} current source. The main advantage of this circuit depends on the performance of CCII, which has wide bandwidth obtained with relatively low biasing currents.

The current conveyor was defined as a three-port device. If a voltage is applied to terminal Y, an equal potential will appear on the input terminal X. An input current I being forced into the terminal X will result an equal amount of current flowing into terminal Y. The current I will be conveyed to output terminal Z such that terminal Z has the characteristics of a current source, of value I with high output impedance. Potential of X being set by that of Y, is independent of the current being forced into port X.

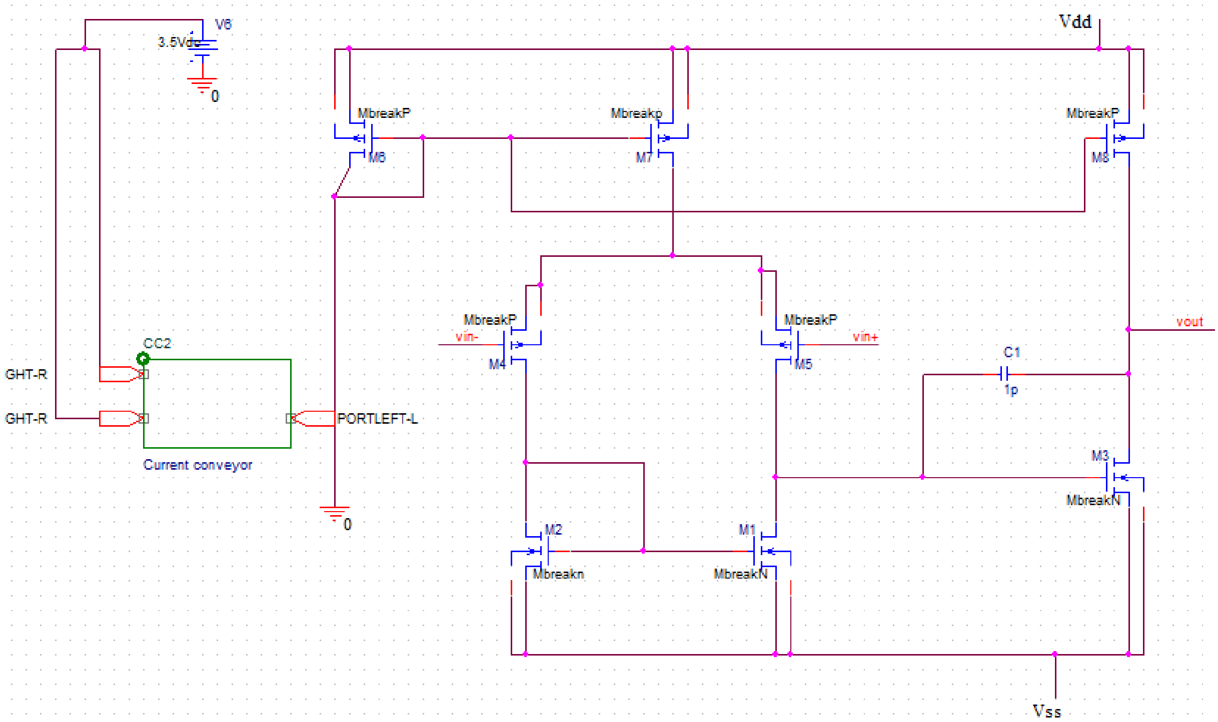

Fig. 4 CCII based OTA circuit

Transistor	W /L(μm)
M1,M2	15/1
M4,M5	24/1
M6,M7	46/1
M3	150/1
M8	230/1

Table 2: CCII+ based OTA Transistor Dimension

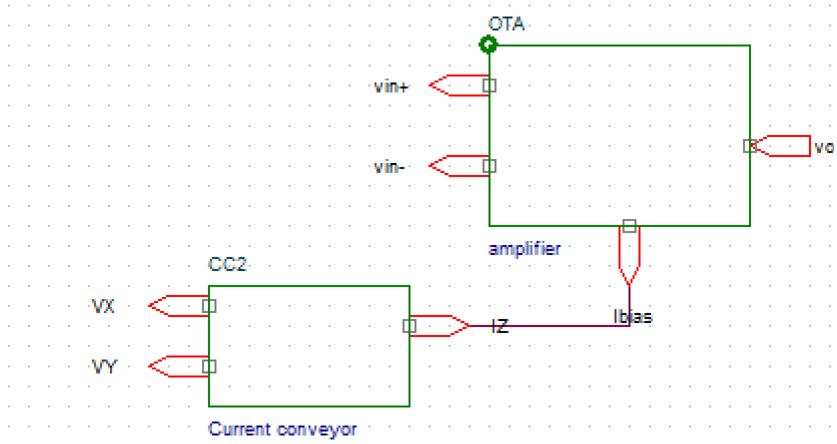

Fig.5 Equivalent circuit diagram of CCII+ based OTA

III. SIMULATION RESULTS AND COMPARISONS

The simulated results of transfer function of Miller OTA and CCII+ based OTA are shown in Fig.6 and Fig.7

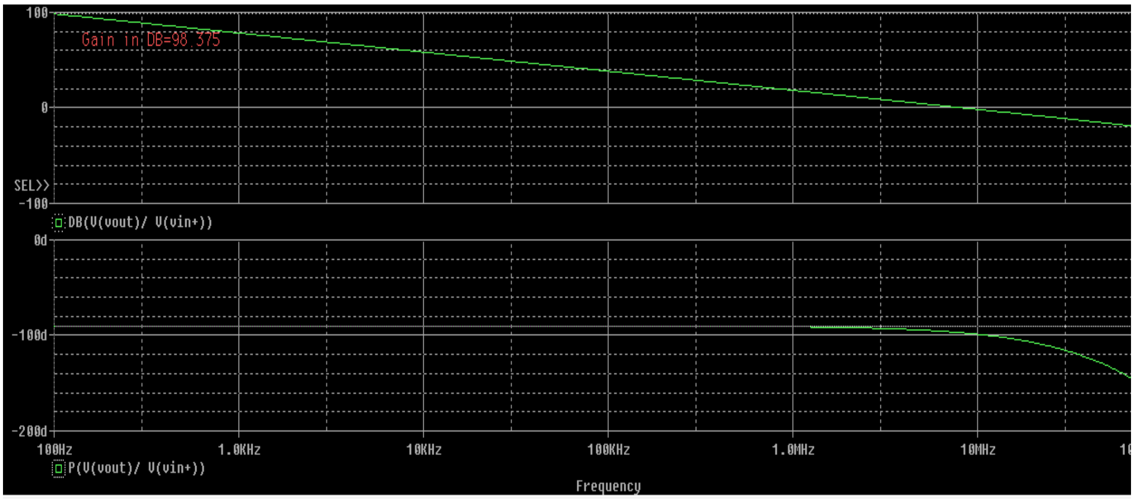

Fig.6 -Simulated transfer function of Miller OTA

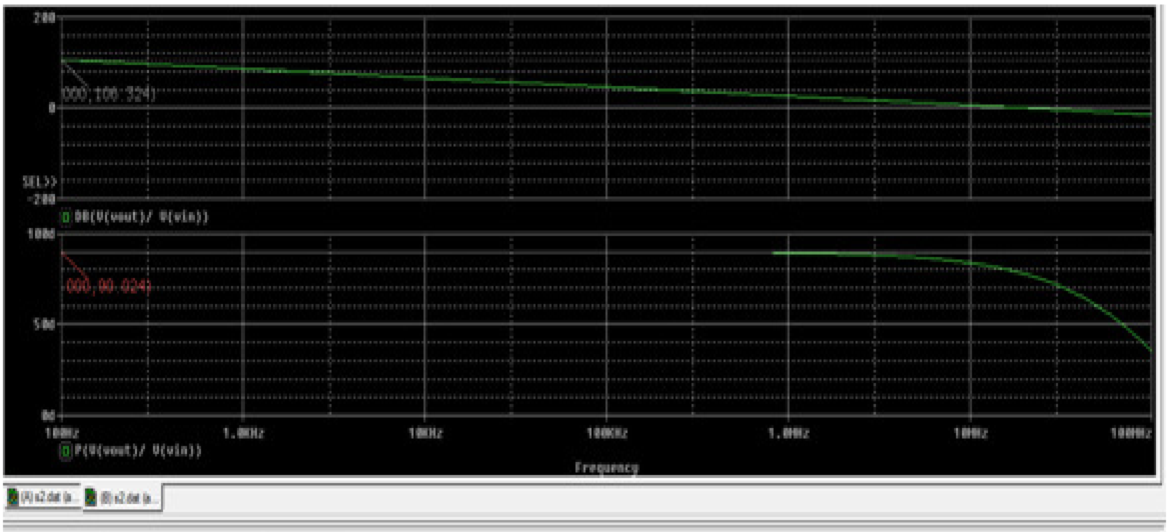

Fig.7 - Simulated transfer function of Current Conveyor based OTA

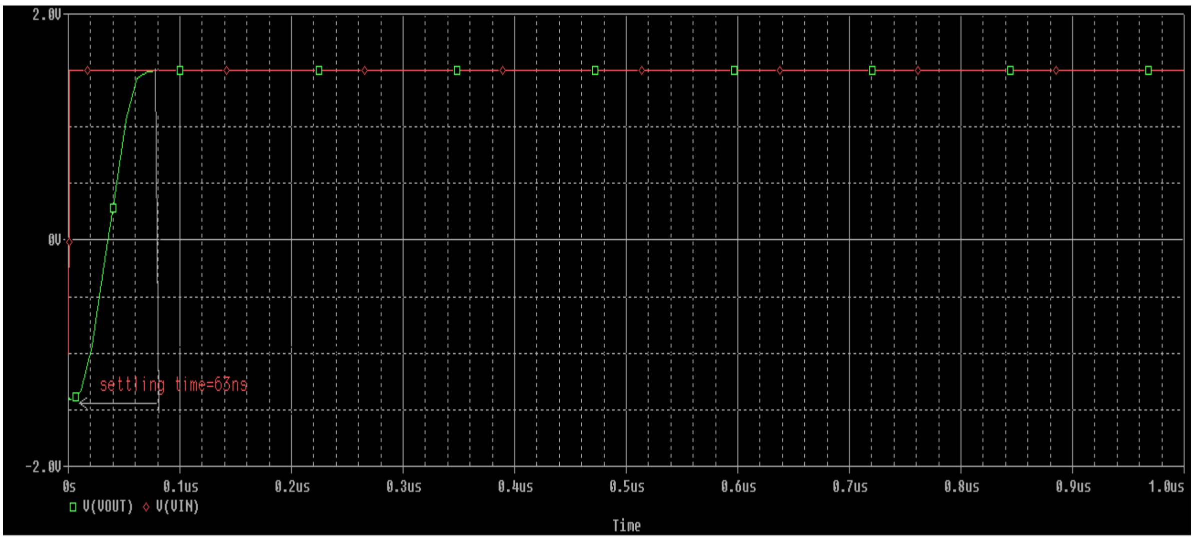

Fig.8 Graphical representation of settling time of Miller OTA

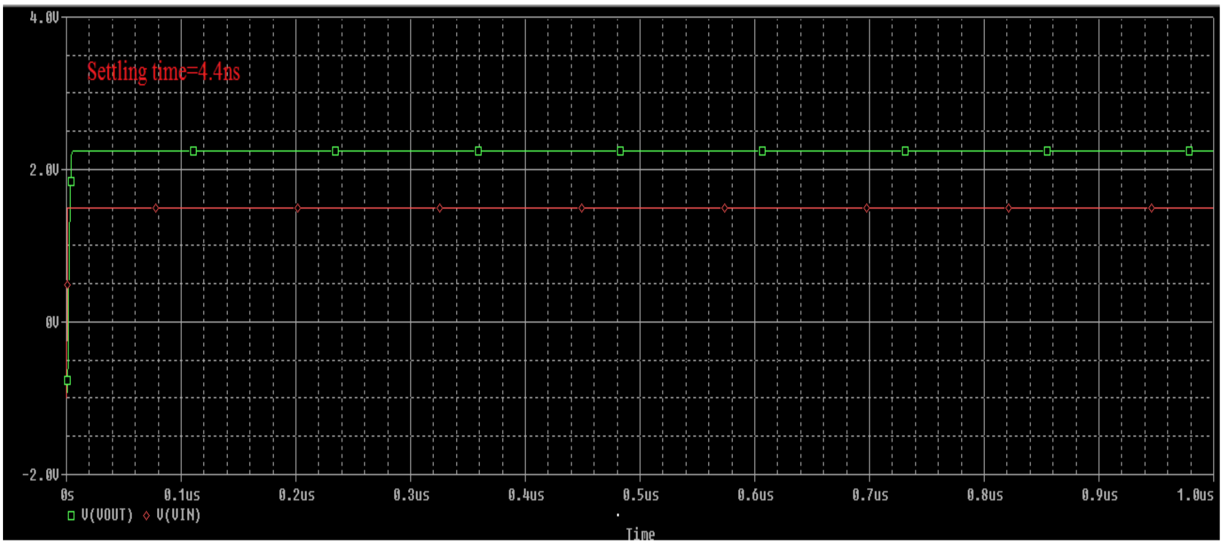

Fig.9 Graphical representation of settling time of CCII+ based OTA

Table 3- Comparison of simulated results of the Miller OTA and Current conveyor based OTA

Parameters	Two stage Miller OTA	CCII+based OTA
Technology	AMS .35 µm technology	AMS .35 µm technology
Dc Gain	98dB	106dB
Phase Margin	82.74°	91°
Power consumption	3.5 mW	2.74µW
Settling Time (Desired band=2%)	63ns	4.4ns
Supply voltage	1.5V	1.5V

IV. CONCLUSION

Design of OTA is very important in analog and mixed signal systems as there is a great need of high gain, low power consumption and high speed, to improve the circuit performance In this paper the goal to reach high gain and high speed has been fulfilled. Behavioral simulations indicated that gain has been increased up to 106 dB. The design technique proposed in this paper combines better performance with simplicity of design related to modifications in Miller OTA. Future work would involve the addition of third generation current conveyor in place of I_{bias} which will increase the gain bandwidth product and reduce power consumption which are the basic need of today's analogue circuit.

V. REFERENCES

1. K. Smith, A. Sedra, "The current-conveyor - a new circuit building block", IEEE Proc., vol. 56, pp. 1368-69, 1968.
2. A. Sedra, K. Smith, "A second-generation current-conveyor and its applications", IEEE Trans., vol. CT-17, pp.132-134, 1970
3. A. Fabre, "Third-generation current conveyor: a new helpful active element", Electronics Letters, vol. 31, pp. 338-339, March 1995.
4. Houda Daoud, samir Ben Salem, Sonia Zouari, Mourad Louiou "Folded cascode OTA for Wide Band Applications"IEEE 2006

5. Mr.Bhavesh H.Soni, Ms.Rasika N.Dhavse “Design Operational Transconductance Amplifier Using 0.35µm Technology” International Journal of Wisdom Based Computing, Vol.1 (2), August 2011)
6. Radwene Laajimi, Nawfil Gueddah, Mohamed Masmoudi A novel design method of two stage CMOS OTA used for wireless sensor receiver(Published in International journal of computer applications, volume 39,no-11,feb 2012)-Technological specification of OTA.
7. David Johns and Kenneth W. Martin: "Analog Integrated Circuit Design" John Wiley & Sons, 1997.
8. E.J, Duarte-Melo and Mingyan Liu: "Analysis of energy consumption and lifetime of heterogeneous wireless sensor networks," Global Telecommunications Conference, 2002G LOBECOM ’02. IEEE, vol.1, no., 17-21 Nov 2002.
9. Mohammed Arifuddin Sohel, Dr. K. Chennakeshava Reddy and Dr. Syed Abdul Sattar, “Linearity Enhancement of Operational Transconductance Amplifier Using Source Degeneration” International Journal of Advanced Research in Engineering & Technology (IJARET), Volume 4, Issue 3, 2012, pp. 257 - 263, ISSN Print: 0976-6480, ISSN Online: 0976-6499.
10. Rajinder Tiwari, R K Singh, “An Optimized High Speed Dual Mode CMOS Differential Amplifier for Analog Vlsiapplications” International Journal of Electrical Engineering & Technology (IJEET), Volume 3, Issue 1, 2012, pp. 180 - 187, ISSN Print: 0976-6545, ISSN Online: 0976-6553.
11. S. S. Khot, P. W. Wani,M. S. Sutaone and S.K.Bhise, “A 555/690 MSPS 4-Bit CMOS Flash ADC Using TIQ Comparator” International Journal of Electrical Engineering & Technology (IJEET), Volume 3, Issue 2, 2012, pp. 373 - 382, ISSN Print: 0976-6545, ISSN Online: 0976-6553.
12. S. S. Khot, P. W. Wani, M. S. Sutaone and S.K.Bhise, “A Low Power 2.5 V, 5-BIT, 555-MHZ Flash ADC In 0.25M Digital CMOS” International journal of Computer Engineering & Technology (IJCET), Volume 3, Issue 2, 2012, pp. 533 - 542, ISSN Print: 0976 – 6367, ISSN Online: 0976 – 6375.